

WHAT IS CLAIMED IS:

1. A method for manufacturing a tantalum oxy  
nitride capacitor comprising:

*Sub A17*  
forming a lower electrode on a surface of a  
semiconductor substrate using a material selected  
from the group consisting of undoped silicon, doped  
silicon and mixtures thereof;

forming MPS (Metastable Poly Silicon) using  
gases each containing a silicon source after  
10 performing wet etching or dry etching of the lower  
electrode;

performing MPS doping in a chamber by using a  
mixed gas comprising P;

depositing a nitride film, in said chamber;

15 depositing a tantalum oxy nitride thin film  
using a chemical vapor comprising tantalum on the  
nitride film;

performing nitrating or nitrifying a surface of  
the tantalum oxynitride thin film; and

20 forming an upper electrode by stacking a metal  
layer on an upper portion of the tantalum oxy  
nitride thin film.

2. The method for manufacturing a tantalum oxy  
25 nitride capacitor according to claim 1, wherein the MPS  
formation, the MPS doping, the nitride depositing and the  
tantalum oxy nitride film depositing are performed in  
said chamber.

30 3. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 1, wherein the wet  
etching or the dry etching of the lower electrode is  
performed using a gas comprising HF.

4. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 1, wherein the gas  
comprising HF is selected from the group consisting of  
hydrogen fluoride/water ( $\text{HF}/\text{H}_2\text{O}$ ), hydrogen  
5 fluoride/hydrogen peroxide ( $\text{HF}/\text{H}_2\text{O}_2$ ), buffered oxide  
etchant (BOE), hydrogen fluoride/acetic acid/nitrogen  
dioxide ( $\text{HF}/\text{CH}_3\text{COOH}/\text{NO}_2$ ) and mixtures thereof.

5. The method for manufacturing a tantalum oxy  
10 nitride capacitor according to claim 1, wherein the gas  
comprising a silicon source is used in the MPS formation  
selected from the group consisting of  $\text{SiH}_4$ ,  $\text{Si}_2\text{H}_6$ ,  $\text{SiH}_2\text{Cl}_2$   
and mixtures thereof.

15 6. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 1, wherein the MPS  
doping is performed under a pressure ranging from about  
 $1.0 \times 10^{-3}$  to about 500 torr and at a temperature ranging  
from about 500 to about 1000°C.

20 7. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 1, wherein the gas  
comprising P is a mixed gas comprising  $\text{PH}_3$ .

25 8. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 7, wherein the mixed  
gas comprising  $\text{PH}_3$  is selected from the group consisting  
of  $\text{PH}_3/\text{N}_2$ ,  $\text{PH}_3/\text{H}_2$ ,  $\text{PH}_3/\text{SiH}_4$ ,  $\text{PH}_3/\text{Ar}$  and mixtures thereof.

30 9. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 1, wherein the  
nitride depositing is performed by using  $\text{NH}_3$  gas.

10. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 9, wherein the  
nitride depositing is performed under a pressure ranging  
from about 0.1 to about 200 torr and at a temperature  
5 ranging from about 600 to about 850°C.

11. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 1, wherein the  
evaporated tantalum ethylate is the chemical vapor  
10 comprising tantalum.

12. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 1, wherein the  
tantalum oxy nitride postprocessing is performed by  
15 nitrating the surface under  $\text{NH}_3$  (or  $\text{N}_2/\text{H}_2$ ) atmosphere or  
nitrifying the surface under  $\text{N}_2\text{O}$  or  $\text{O}_2$  atmosphere.

13. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 1, wherein the  
20 nitrating or nitrifying is performed at a temperature  
ranging from about 200 to about 600°C by using a plasma.

14. The method for manufacturing a tantalum oxy  
nitride capacitor according to claim 1, wherein the upper  
25 electrode is formed by depositing a material selected  
from the group consisting of poly silicon (Poly Si),  
titanium nitride (TiN), tantalum nitride (TaN), tungsten  
(W), tungsten nitride (WN), tungsten silicide (Wsi),  
ruthenium (RU), ruthenium oxide ( $\text{RuO}_2$ ), iridium (Ir),  
30 platinum (Pt), individually or repeatedly to form a  
stacking structure.

15. A semiconductor device comprising a capacitor  
made in accordance with the method of claim 1.

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